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(54) Method of fabricating a surface coupled InGaAs photodetector

(57) A photodetector is fabricated in a multilayer structure having a semi-insulating InP substrate (22), an n+ InP contact layer (24) overlying the InP substrate (22), an undoped InGaAs (26) absorbing layer overlying the n+ InP contact layer (24), and a p+ doped InGaAs layer (28) overlying the undoped InGaAs absorbing layer (26). A gold-beryllium p-contact dot (30) is deposited onto the p+ doped InGaAs layer (28) of the multilayer structure. A mesa structure is etched with a citric acid-based etchant into the multilayer structure. The mesa structure includes the metal p-contact dot (30), the p+ doped InGaAs layer (28), and the undoped InGaAs absorbing layer (26). The n+ InP contact layer (24) is patterned, and a passive metallic n-contact layer (32) is deposited onto the patterned n+ InP contact layer (24). A polyimide insulator layer (34) overlying a portion of the structure is deposited and patterned, so that the polyimide insulator layer (34) does not cover the passive metal p-contact dot (30) and the metallic n-contact layer (32). The patterned organic polymer insulator layer (34) is cured and the device is passivated by heating it in a nitrogen atmosphere. Thick metallic gold contact traces are deposited, with one trace (36) extending to the gold-beryllium p-contact dot and the other trace (38) extending to the metallic n-contact layer.

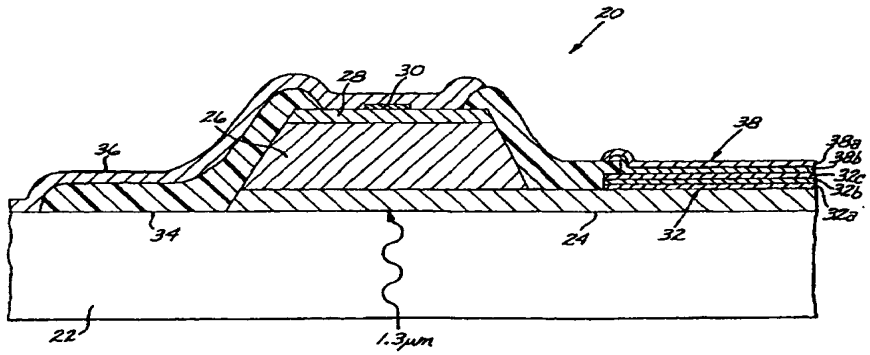

FIG. 1

EP 1 063 709 A2

Description

BACKGROUND OF THE INVENTION

[0001] This invention relates to the fabrication of photodetectors, and, more particularly, to the fabrication of an InGaAs PIN photodetector having high optical-power handling capability with good linearity of conversion to an electrical signal.

[0002] A photodetector is a device that converts incident light into an electrical signal. A light beam is directed onto the photodetector, and the electrical output signal of the photodetector is a measure of the incident energy of the light beam. Photodetectors are available for both visible and infrared light energy.

[0003] Photodetectors are used in a wide variety of applications. For some, the photodetector need only detect the presence of light, and its other component capabilities are not important.

[0004] In other applications, however, the photodetector is used in a signal processing or handling system. The photodetector may act as a part of a signal handling system to convert incident light to an electrical signal for transmission or processing. The photodetector must therefore be capable of handling the desired input power of the light beam, and achieving the conversion to an electrical signal with good linearity, good frequency range, and low distortion.

[0005] A well known photodetector for the near infrared light range is the InGaAs PIN diode. In one version, this diode has a p+ doped InGaAs layer and an n+ InP layer, on either side of an undoped InGaAs layer, with this structure supported on a light-transparent InP substrate. Light incident on the front side of the substrate produces a voltage between the p+ doped InGaAs layer and the n+ InP layer, which voltage is generally proportional to the intensity of the incident light.

[0006] While operable, this InGaAs PIN diode has some shortcomings for particular applications, such as CATV analog transmission systems using RF and microwave antenna networks. For such systems to achieve their best performance, the maximum light intensity must be in the range of greater than 10 milliwatts (mW) of optical signal strength and the light-to-electrical signal conversion must have good linearity. Semiconductor lasers capable of producing an optical signal output in the range of a few tens of milliwatts are now available. However, most existing InGaAs PIN photodiodes are limited to about 2 mW of incident optical signal strength. The systems using the available InGaAs PIN photodiodes therefore cannot take advantage of the capabilities of the higher-power semiconductor lasers. Accordingly, the available photodetectors limit the performance of these systems.

[0007] There is a need for an improved photodetector which can handle high incident optical intensities and convert them to electrical signals with good linearity. The present invention fulfills this need, and further provides related advantages.

SUMMARY OF THE INVENTION

[0008] The present invention provides a fabrication technique for InGaAs PIN diodes. The diodes of the invention are operable to light intensities of greater than 15 mW, with good linearity of conversion to an electrical signal and low noise. The diode is operable over a broad frequency range extending into microwave frequencies. The InGaAs PIN diode of the invention utilizes a known basic structure, with the fabrication processing optimized for good performance.

[0009] In accordance with the invention, a method for fabricating a photodetector, utilizes a multilayer structure comprising a semi-insulating InP substrate, an n+ InP contact layer overlying the InP substrate, an undoped InGaAs absorbing layer overlying the n+ InP contact layer, and a p+ doped InGaAs layer overlying the undoped InGaAs absorbing layer. The method of the invention includes depositing a passive metal p-contact dot onto the p+ doped InGaAs layer of the multilayer structure, and etching a mesa structure into the multilayer structure. The mesa structure includes the passive metal p-contact dot, the p+ doped InGaAs layer, and the undoped InGaAs absorbing layer. The step of etching is performed with an etchant that does not attack the n+ InP contact layer and the InP substrate. The method further includes patterning the n+ InP contact layer, depositing a passive metallic n-contact layer onto the patterned n+ InP contact layer, and depositing a patterned organic polymer insulator layer overlying a portion of the structure. The patterned organic polymer insulator layer does not cover the passive metal p-contact dot and the metallic n-contact layer. The patterned organic polymer insulator layer is thereafter cured, and the device is passivated. Metallic contact traces are deposited, with a first trace extending to the passive metal p-contact dot and a second trace extending to the metallic n-contact layer.

[0010] The preferred multilayer structure includes the approximately 1 micrometer thick InP contact layer that is doped n+ with silicon or tin to a concentration of about 1×10^{19} atoms per cubic centimeter. The absorbing layer is "undoped" InGaAs, where the term "undoped" indicates an absence of intentional doping and a background concentration of less than about 5×10^{15} atoms per cubic centimeter. The doped InGaAs layer is doped p+ with beryllium or zinc to a concentration of about 1×10^{19} atoms per cubic centimeter.

[0011] The passive metal p-contact dot is preferably gold-beryllium metal. The metallic n-contact layer is preferably formed of multiple sublayers, including a gold-germanium layer, a nickel layer, and a gold layer. The organic polymer insulator is preferably a polyimide, which is cured and passivated by heating in a nitrogen atmosphere. The metallic contact traces are preferably thick gold layers, most preferably from about 2.5 to

about 3 micrometers in thickness.

[0012] The mesa structure is etched with an etchant that attacks the InGaAs layers, but not the InP layers. The preferred etchant is based on citric acid, most preferably an aqueous solution of citric acid, hydrogen peroxide, and phosphoric acid.

[0013] Prototypes of the InGaAs PIN photodiode of the invention have been measured to reproducibly produce a highly linear output over a range of light intensities from zero to over 15 mW, and in some cases to as high as 20 mW. The photodiode is operable over a wide bandwidth from dc to 20 GHz. Other performance features of the photodiode are also excellent.

[0014] Other features and advantages of the present invention will be apparent from the following more detailed description of the preferred embodiment, taken in conjunction with the accompanying drawings, which illustrate, by way of example, the principles of the invention. The scope of the invention is not, however, limited to this preferred embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015]

Figure 1 is a schematic sectional view of an InGaAs PIN diode according to the invention;

Figure 2 is a block flow diagram of the preferred method for fabricating the diode of Figure 1;

Figure 3 is a graph of measured photodetector RF point-to-point link loss; and

Figure 4 is a graph of RF power as a function of photocurrent.

DETAILED DESCRIPTION OF THE INVENTION

[0016] Figure 1 depicts a preferred form of an InGaAs PIN diode 20 fabricated according to the invention. The structure is not drawn to scale. The diode 20 includes a substrate 22 made of semi-insulating InP (indium phosphide). The substrate 22 may be of any operable thickness, but is typically about 600 micrometers thick for a 3 inch-diameter wafer. Overlying and contacting the substrate 22 is a doped InP contact layer 24. The contact layer 24 is preferably from about 0.5 to about 1.5 micrometers thick, most preferably about 1 micrometer thick. The contact layer is n+ doped with an element such as Si (silicon) or Sn (tin) in a concentration of from about 5×10^{18} to about 1×10^{19}, preferably about 1×10^{19}, atoms per cubic centimeter.

[0017] Overlying and contacting the contact layer 24 is an absorbing layer 26 of InGaAs (indium gallium arsenide) that is not intentionally doped, termed "undoped" herein. Even though the absorbing layer 26 is not intentionally doped, there is typically a small background concentration of impurity atoms present, usually less than about 5×10^{15} atoms per cubic centimeter. The absorbing layer 26 is preferably from about 0.5 to about 1.5 micrometers thick, most preferably about 1 micrometer thick.

[0018] Overlying and contacting the absorbing layer 26 is a doped InGaAs layer 28. The layer 28 is doped p+ with a dopant such as Be (beryllium) or Zn (zinc). The dopant is present in a concentration of from about 1×10^{19} to about 3×10^{19}, preferably about 1×10^{19}, atoms per cubic centimeter. The layer 28 is preferably from about 0.2 to about 0.6 micrometers thick, most preferably about 0.5 micrometers thick. The layers 24, 26, and 28 together constitute a PIN structure.

[0019] A metallic p-contact of small lateral extent, termed a metallic p-contact dot 30, overlies and contacts the layer 28. The p-contact dot 28 is formed of a passive metal, preferably a Au-Be (gold-beryllium) alloy having a composition in weight percent of about 1.5 percent gold, 98.5 percent beryllium.

[0020] A metallic n-contact 32 overlies and contacts the contact layer 24, at a position laterally separated from the p-contact dot 30. The n-contact 32 is preferably in the form of a layer having a thickness of about 4000 Angstroms. The n-contact is made of a passive metal combination. A most preferred n-contact 32 includes a gold-germanium sublayer 32a (having a composition by weight of about 88 percent gold, about 12 percent germanium) overlying and contacting the layer 24, a nickel sublayer 32b overlying and contacting the layer 32a, and a gold sublayer 32c overlying and contacting the layer 32a.

[0021] A passive organic polymer insulator layer 34, preferably comprising a polyimide, overlies the structure just described, except for openings therethrough exposing the dot 30 and at least a portion of the n-contact 32.

[0022] A first metallic contact trace 36 extends to the p-contact dot 30, and a second metallic contact trace 38 extends to the n-contact layer 32. The traces 36 and 36 are preferably formed as a thick Au (gold) layer 38a from about 2.5 to about 3.0 micrometers thick overlying a thin Ti-Au (titanium-gold) plating plane layer 38b. These traces 36 and 38 are relatively thick at about 2.5-3.0 micrometers. This thickness of trace allows increased current flow and also aids in heat dissipation, both of which improve the ability of the diode to handle high optical intensities. For these reasons, even thicker traces 36 and 38 would be desirable.

[0023] When illuminated through the substrate 22 by light in the near infrared (e.g., about 1.3 micrometer wavelength), the PIN structure produces a potential difference and current that are transmitted through the traces 36 and 38 to external measurement apparatus, not shown.

[0024] Figure 2 depicts a preferred approach for fabricating the diode 20 depicted in Figure 1. Steps 50, 52, 54, and 56 set forth a method for preparing the multilayer structure of layers 22, 24, 26, and 28. The InP substrate 22 is provided, numeral 50. The n+ InP contact layer 24 is deposited overlying and in contact with the substrate 22, numeral 52. The InGaAs absorbing

layer 26 is deposited overlying and in contact with the contact layer 24, numeral 54. The p+ InGaAs layer 28 is deposited overlying and in contact with the absorbing layer 26, numeral 56. The InP substrate 22 is available commercially. Each of the layers has the thickness, composition, dopants, and other features discussed above in relation to Figure 1. Each of the depositing steps 52, 54, and 56 may be performed by any operable deposition technique, preferably molecular beam epitaxy (MBE) or metal oxide vapor phase epitaxy (MOVPE). Such deposition techniques are well known in the art for other applications.

[0025] The diode 20 is fabricated from this basic multilayer structure, as depicted in steps 58-70. To fabricate the diode, the p-contact dot 30 is deposited, numeral 58. The deposition is accomplished by patterning the upper side of the layer 28 using conventional photolithography techniques, and depositing the metal that forms the dot 30 through openings in the pattern. Photolithography is preferably used for this and succeeding steps of patterning, depositing, and etching, because in a typical case there will be many diodes 20 fabricated on the same InP substrate 22. The dots 30 are preferably formed of Au-Be alloy, deposited by thermal evaporation. Each dot 30 is typically about 28 micrometers in diameter and 1000 Angstroms thick.

[0026] The resulting structure is mesa etched, numeral 60. In mesa etching, the exposed upper surface of the structure is patterned using conventional photolithography techniques, leaving a protective layer overlying the dot 30 and surrounding area in a total diameter of about 30 micrometers. The remaining unprotected portions of the layers 28 and 26, both InGaAs, are etched away. The etchant is preferably a citric acid-based etchant, most preferably a solution of water, 1 molar citric acid, 30 percent aqueous solution of hydrogen peroxide, and 85 percent aqueous solution of phosphoric acid in a volume ratio of 220:55:5:1. This etchant is selective, in that it removes only the exposed InGaAs, and stops when it encounters the InP layer 24.

[0027] The n+ InP layer 24 is patterned to isolate the mesas of adjacent diodes 20 and to define an area for electrode attachment to layer 24 using conventional photolithography techniques, numeral 62. The etching is preferably accomplished using a solution of water, 48 percent aqueous solution of hydrogen bromide and 30 percent aqueous solution of hydrogen peroxide in a volume ratio of 100:250:2.

[0028] The n-contact layer 32 is deposited onto the patterned n+ InP layer 24, numeral 64, using conventional photolithography techniques. The n-contact layer is preferably deposited as three overlying sublayers. The Au-Ge sublayer 32a is deposited overlying and in contact with the layer 24, to a thickness of 900 Angstroms. The Ni sublayer 32b is deposited overlying and in contact with the layer 32a, to a thickness of 100 Angstroms. The gold sublayer 32c is deposited overlying and in contact with the layer 32b, to a thickness of 3000 Angstroms.

[0029] The polymeric insulating layer 34 is deposited overlying portions of the exposed surface and thereafter cured and passivated, numeral 66. The deposition is accomplished using conventional photolithography techniques. For this purpose, the polymer is preferably a photosensitive polyimide such as Probimide 7505 available from Olin Microelectronic Materials. The polymer is deposited overlying all areas of the exposed surface, except for the p-contact dot 30 and the n-contact layer 32, leaving at least some of these regions exposed. The polymer is deposited by spin coating and standard photolithographic definition. After deposition, the polymer must be cured by heating. To simultaneously cure the polymer and passivate the device, it is heated to an appropriate curing temperature in a pure nitrogen atmosphere. For the preferred polyimide, the curing is accomplished at a temperature of 350°F and for a time of 1 hour.

[0030] The metallic contact traces 36 and 38 are deposited so as to reach to the respective p-contact dot 30 and the n-contact layer 32, numeral 68. Because the traces are relatively thick, they are preferably deposited by electroplating. To permit electroplating over the insulating polymer layer 34, a titanium-gold plating plane layer 38b is first deposited by a technique such as sputtering, to a thickness of about 200 Angstroms of titanum and 1000 Angstroms of gold, over the entire exposed surface of the structure. The upper surface is then patterned using conventional photolithography techniques with openings defining the traces 36 and 38. Using the plating plane layer 38b as the electrical contact, the remaining thicknesses of the traces 36 and 38 are deposited by electroplating a gold layer 38a to a thickness of from about 2.5 to about 3.0 micrometers through the openings of the photoresist.

[0031] Lastly, any exposed portion of the titanium-gold plating plane layer 38b is removed, numeral 70, preferably by ion milling. The upper surface of the layer 34 is thereby exposed, so that the exposed surface is insulating except for the traces 36 and 38.

[0032] The result is the diode 20 illustrated in Figure 1.

[0033] Diodes prepared according to the present approach have been fabricated and tested. Figure 3 illustrates the measured RF point-to-point link loss for the diode of the invention as compared with a conventional commercial InGaAs PIN diode. The link loss of the diode 20 of the invention is approximately constant as a function of current output (and thence light input) of the diode, a desirably feature, while the link loss for a commercial diode increases substantially with increasing current. Figure 4 illustrates that the output power as a function of photocurrent is nearly linear for each of the fundamental and the first three harmonics. All of the measurements are highly linear in form, and all of the harmonics are less than 60 dB at 5 mA of photocurrent over the frequency band of 15 GHz. The third intercept

of the photodetector was measured to be 22 dBm. Additionally, the dc current voltage characteristics and the capacitance of the photodetector measured at -5V are less than 10 nanoamperes with a breakdown voltage of less than 20 volts, and 100 fF, respectively. The dc responsivity of the photodetector is 0.8 A/W.

[0034] Although a particular embodiment of the invention has been described in detail for purposes of illustration, various modifications and enhancements may be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be limited except as by the appended claims.

Claims

1. A method for fabricating a photodetector (20), comprising the steps (50, 52, 54, 56) of furnishing a multilayer structure comprising

   a semi-insulating InP substrate (22),
   an n+ InP contact layer (24) overlying the InP substrate (22),
   an undoped InGaAs absorbing layer (26) overlying the n+ InP contact layer (24), and
   a p+ doped InGaAs layer (28) overlying the undoped InGaAs absorbing layer (26);
   depositing (58) a metal p-contact dot (30) onto the p+ doped InGaAs layer (28) of the multilayer structure;
   etching (60) a mesa structure into the multilayer structure, the mesa structure including the passive metal dot (30), the p+ doped InGaAs layer (28), and the undoped InGaAs absorbing layer (26), the step of etching (60) including the step of utilizing an etchant that does not attack the n+ InP contact layer (24) and the InP substrate (22);
   patterning (62) the n+ InP contact layer (24);
   depositing (64) a passive metallic n-contact layer (32) onto the patterned n+ InP contact layer (24);
   depositing (66) a patterned organic polymer insulator layer (34) overlying a portion of the structure, the patterned organic polymer insulator layer (34) not covering the passive metal dot (30) and the metallic n-contact (32);
   curing (66) the patterned organic polymer insulator layer (34); and
   depositing (68) metallic contact traces (36, 38) to the p-contact dot (30) and the n-contact layer (32).

2. The method of claim 1, characterized in that the step of furnishing includes the step of furnishing the multilayer structure wherein

   the n+ InP contact layer (24) is doped with a concentration of about 1 x 10^{19} atoms per cubic centimeter of a dopant selected from the group consisting of Si and Sn.

3. The method of claim 1 or 2, characterized in that the step of furnishing includes the step of furnishing the multilayer structure wherein

   the p+ doped InGaAs layer (28) is doped with a concentration of about 1 x 10^{19} atoms per cubic centimeter of a dopant selected from the group consisting of beryllium and zinc.

4. The method of any of the preceding claims, characterized in that the step of depositing the passive metal dot (30) includes the step of

   depositing a gold-beryllium metal dot.

5. The method of any of the preceding claims, characterized in that the step (60) of etching a mesa structure includes the step of

   etching using an aqueous solution of citric acid, hydrogen peroxide, and phosphoric acid.

6. The method of any of the preceding claims, characterized in that the step (62) of patterning the n+ InP contact layer (24) includes the step of

   etching the n+ InP contact layer (24) with an aqueous solution of hydrogen bromide and hydrogen peroxide.

7. The method of any of the preceding claims, characterized in that the step (64) of depositing a passive metallic n-contact (32) includes the step of

   depositing the contact with a gold-germanium sublayer (32a), a nickel sublayer (32b), and a gold sublayer (32c).

8. The method of any of the preceding claims, characterized in that the step (66) of depositing a patterned organic polymer insulator layer (34) includes the step of

   depositing a polyimide.

9. The method of any of the preceding claims, characterized in that the step (66) of curing includes the step of

   heating the polymer insulator layer (34) in a nitrogen atmosphere.

10. The method of any of the preceding claims, characterized in that the step (68) of depositing metallic contact traces (36, 38) includes the step of

depositing a titanium-gold sublayer (38b), and thereafter

depositing a gold layer (38a) having a thickness of from about 2.5 to about 3 micrometers.

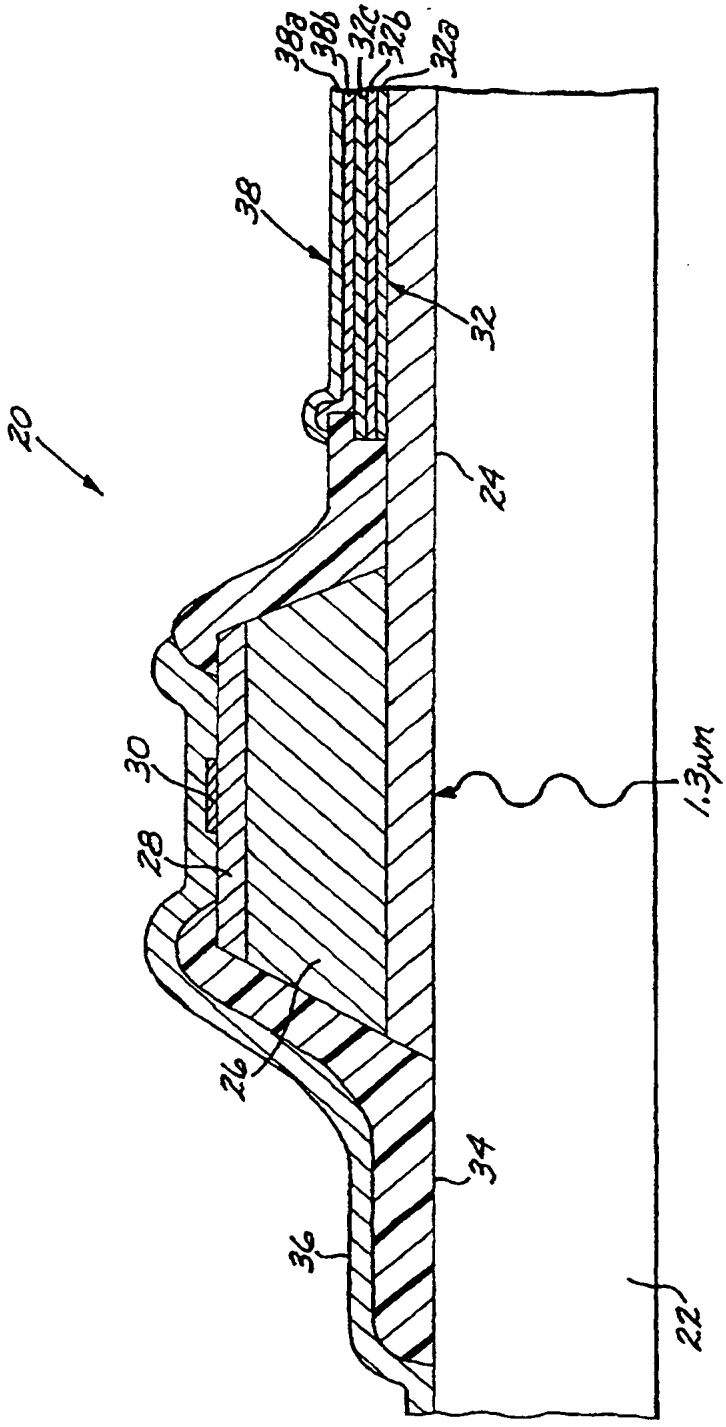

FIG. 1

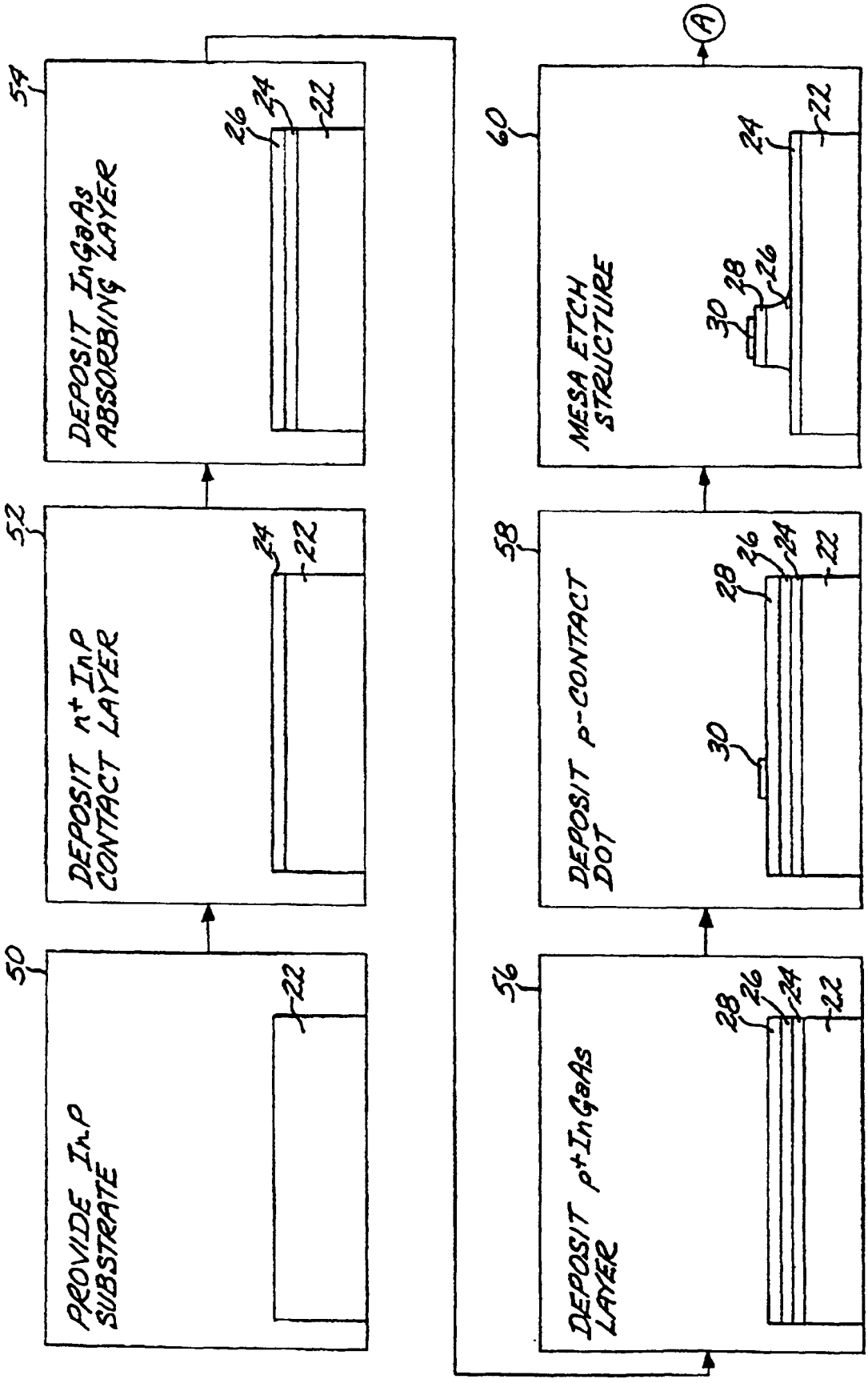
50
PROVIDE InP SUBSTRATE
22
52
DEPOSIT n+ InP CONTACT LAYER
24
22
54
DEPOSIT InGaAs ABSORBING LAYER
26
24
22
56
DEPOSIT p+InGaAs LAYER
28
26
24
22
58
DEPOSIT p-CONTACT DOT
30
28
26
24
22
60
MESA ETCH STRUCTURE
30
28
26
24
22
A

FIG. 2 (SHEET 1)

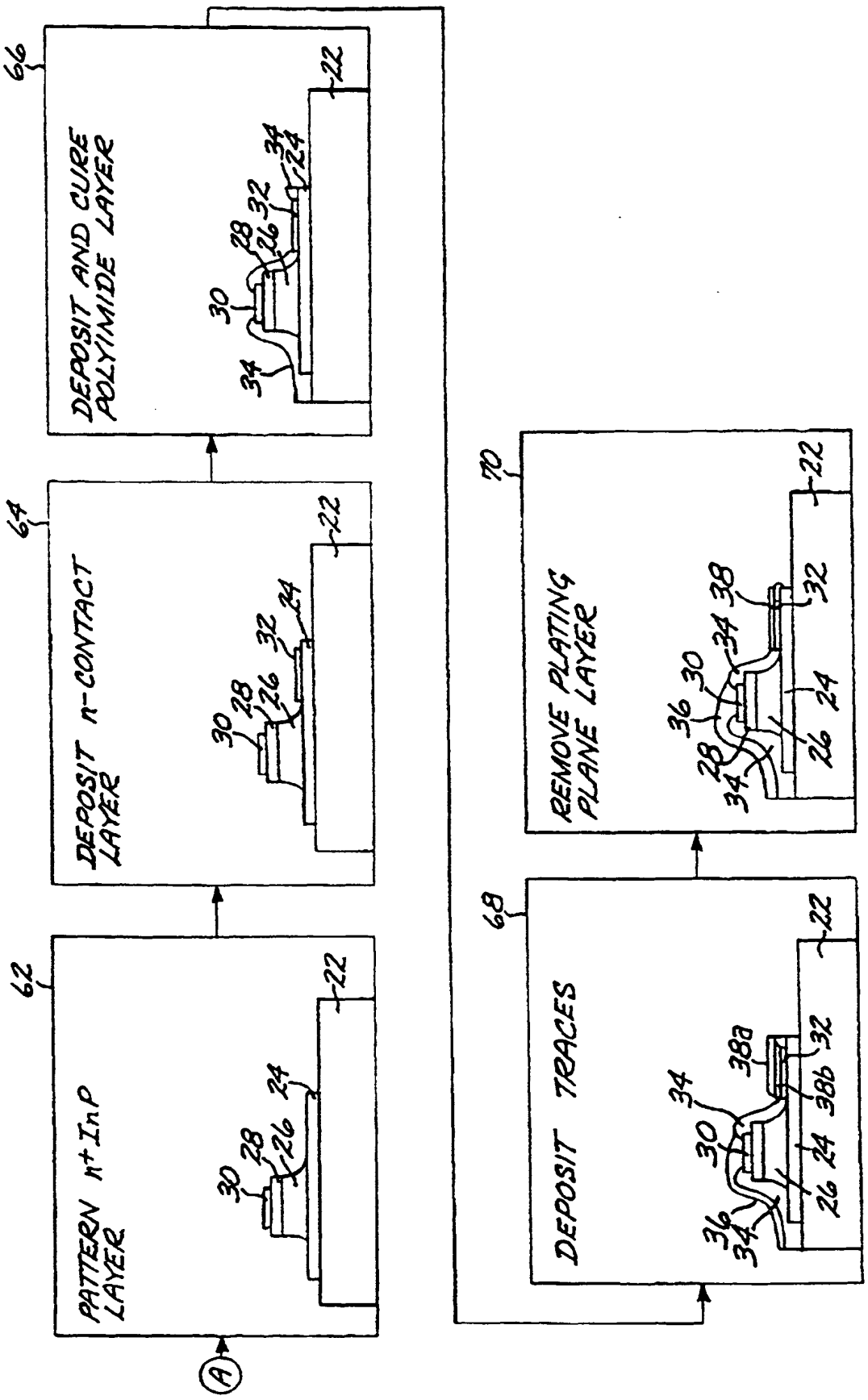
62
PATTERN n+ InP LAYER
64
DEPOSIT n-CONTACT LAYER
66
DEPOSIT AND CURE POLYIMIDE LAYER
68
DEPOSIT TRACES
70
REMOVE PLATING PLANE LAYER
A
22
24
26
28
30
32
34
36
38a
38b

FIG. 2 (SHEET 2)

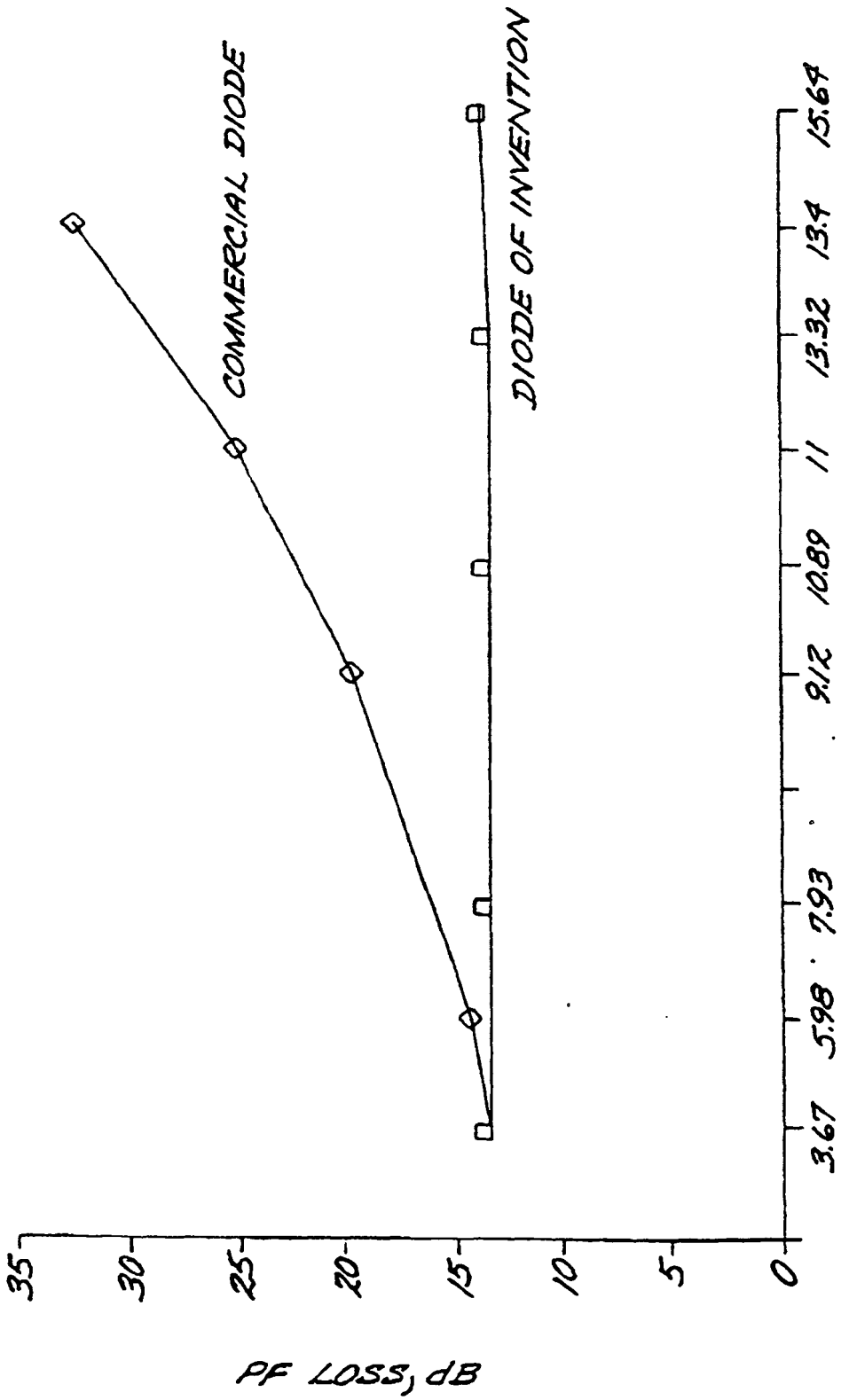
COMMERCIAL DIODE
DIODE OF INVENTION
RF LOSS, dB
35
30
25
20
15
10
5
0
3.67
5.98
7.93
9.12
10.89
11
13.32
13.4
15.64
PHOTODETECTOR CURRENT, mA

FIG. 3

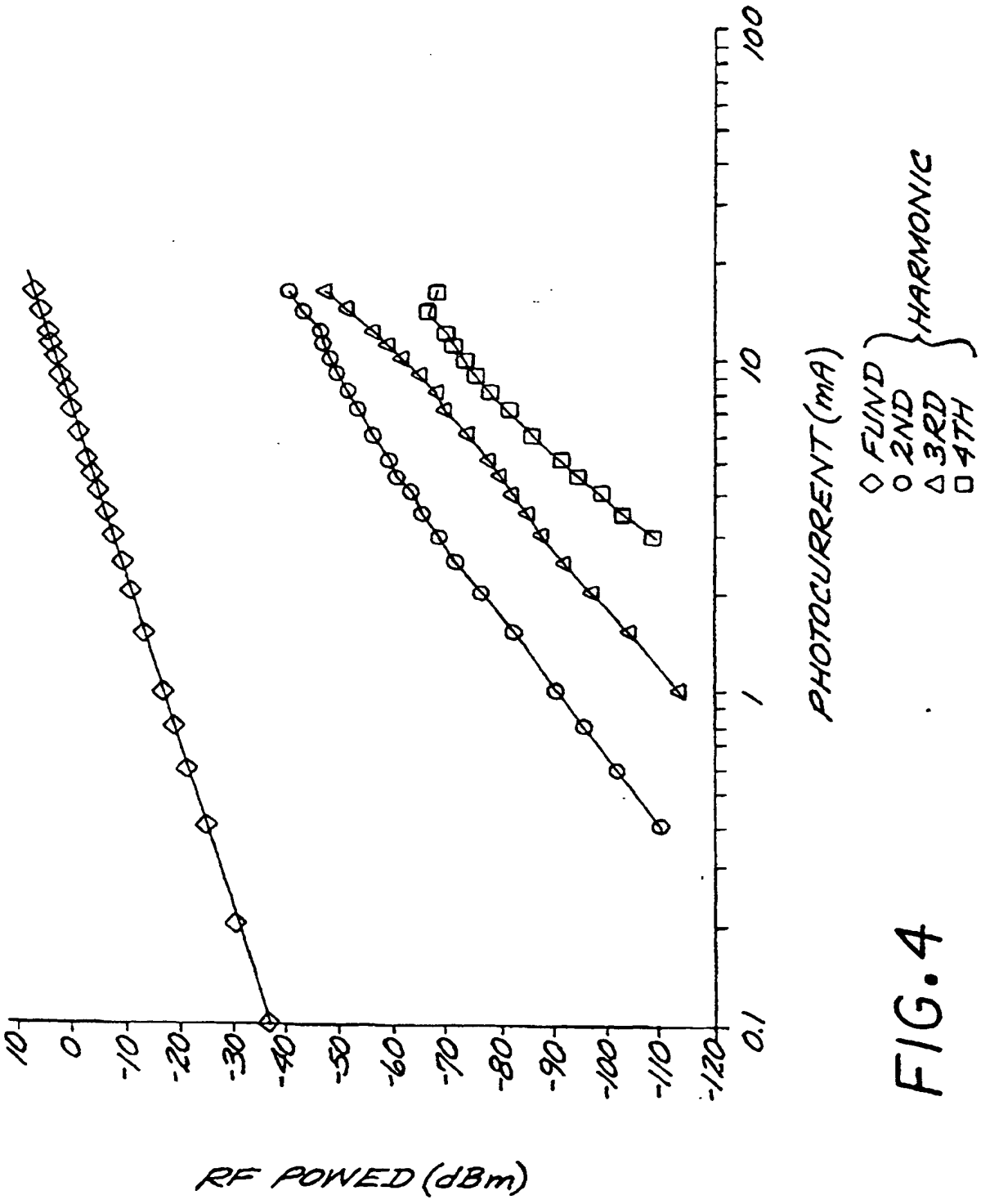
10
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
RF POWED (dBm)
0.1
1
10
100
PHOTOCURRENT (mA)
◇ FUND
○ 2ND
△ 3RD
□ 4TH
HARMONIC

FIG. 4

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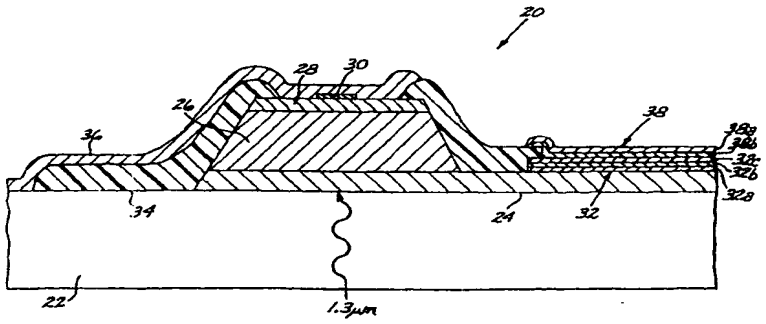

FIG. 1

EP 1 063 709 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 10 9952

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	WEY Y -G ET AL: "110-GHZ GAINAS/INP DOUBLE HETEROSTRUCTURE P-I-N PHOTODETECTORS" JOURNAL OF LIGHTWAVE TECHNOLOGY,US,IEEE. NEW YORK, vol. 13, no. 7, 1 July 1995 (1995-07-01), pages 1490-1499, XP000597674 ISSN: 0733-8724	1-3,7-10	H01L31/18 H01L31/0304 H01L31/105
Y	* the whole document *	4-6	
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